CLAIMS

1. A semiconductor device comprising:

a) a source, a drain and a body between the source and the drain, the body having a first side and a second side;

b) a first double gate, the first double gate having a first portion adjacent to the body first side and a second portion adjacent to said body second side;

c)a second double gate, the second double gate having a first portion adjacent to the body first side and a second portion adjacent to said body second side.

2. The semiconductor device of claim 1 wherein the body comprises a fin body that has a width narrow enough to insure a fully depleted channel during operation of the transistor.

3. The semiconductor device of claim 1 wherein the first double gate receives a first control signal and said second double gate receives a second control signal.

4. The semiconductor device of claim 1 wherein the body comprises a portion of a silicon-on-insulator layer.

5. The semiconductor device of claim 1 further comprising an insulating spacer between the first double gate and the second double gate.

6. The semiconductor device of claim 1wherein the first body side and the second body side are on opposite sides of the body.

7. The semiconductor device of claim 1 comprising a first insulating spacer between the first portion of the first double gate and the first portion of the second double gate, and a second insulating spacer between the second portion of the first double gate and the second portion of the second double gate.

8. The semiconductor device of claim 7 wherein the first insulating spacer and second insulating spacer are formed offset such that the first insulating spacer and second insulating spacer are not inline across the body.

9. A method for forming a field effect transistor, the method comprising the steps of:

a) providing a semiconductor substrate;

b) patterning the semiconductor substrate to provide a body, the body having a first side and a second side;

c) forming a first double gate, the first double gate having a first portion adjacent to the body first side and a second portion adjacent to said body second side;

d) forming a second double gate, the second double gate having a first portion adjacent to the body first side and a second portion adjacent to the said body second side.

10. The method of claim 9 wherein the step of patterning the semiconductor substrate to provide a body comprises patterning the semiconductor substrate to form a fin type body.

11. The method of claim 9 wherein the semiconductor substrate comprise a silicon-on-insulator layer and wherein the step of patterning the semiconductor substrate to provide a body comprises patterning the silicon-on-insulator layer.

12. The method of claim 9 further comprising the step of forming an insulating spacer between the first double gate and the second double gate.

13. The method of claim 12 wherein the step of forming an insulating spacer between the first double gate and the second double gate comprises forming a first insulating spacer between the first portion of the first double gate and the first portion of the second double gate, and forming a second insulating spacer between the second portion of the first double gate and the second portion of the second double gate, wherein the first insulating spacer and second insulating spacer are formed offset such that the first insulating spacer and second insulating spacer are not inline across the body.

14. The method of claim 9 further comprising the steps of forming a contact on the first double gate to provide a first control signal and a contact on the second double gate to provide a second control signal.

15. A transistor comprising:

a) a fin body formed on a substrate, the fin body having a first vertical edge and a second vertical edge, and a first end and a second end;

b) a source formed at the first end of the fin body, and a drain formed at the second end of the fin body;

c) a first gate structure adjacent the transistor body first vertical edge and second vertical edge, the first gate structure approximate to the source; and

d) a second gate structure adjacent the transistor body first vertical edge and second vertical edge, the second gate structure approximate to the drain.

16. The transistor of claim 15 further comprising a spacer between the first gate structure and the second gate structure.

17. The transistor of claim 16 wherein the portion of the spacer adjacent to the first vertical edge is offset from the portion of the spacer adjacent to the second vertical edge.

18. The transistor of claim 15 wherein the fin body has a width narrow enough to insure a fully depleted channel during operation of the transistor.

19. The transistor of claim 15 wherein a portion of the first gate structure adjacent to the first vertical edge of the transistor body is directly opposite a portion of the second gate structure adjacent to the second vertical edge of the transistor body.

20. The transistor of claim19 wherein the first gate structure adjacent to the first vertical edge off the transistor body has a work function which is more attractive to dominant charge carriers of the transistor compared to that of the first gate structure adjacent to the second vertical edge of the transistor body.

21. The transistor of claim 20 wherein the second gate structure adjacent to the second vertical edge of the transistor body has a work function which is more attractive to the dominant charge carriers of the transistor compared to that of the second gate structure adjacent to the first vertical edge of the transistor body.

22. The transistor of claim 15 wherein an edge of the first gate structure adjacent to the first vertical edge of the transistor body is opposite, and displaced less than the body thickness from an edge of the second gate structure adjacent to the second vertical edge of the transistor body

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